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74LVT574, 74LVTH574
Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH574), also available without bushold feature (74LVT574)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32mA/+64mA
- Functionally compatible with the 74 series 574
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

General Description

The LVT574 and LVTH574 are high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

The LVTH574 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT574 and LVTH574 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

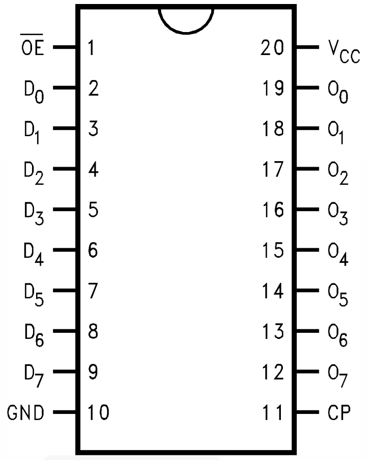
Ordering Information

Order Number	Package Number	Package Description
74LVT574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVT574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVT574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVTH574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



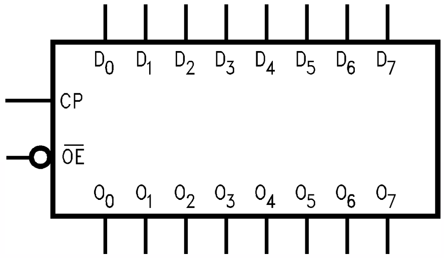
Pin Description

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

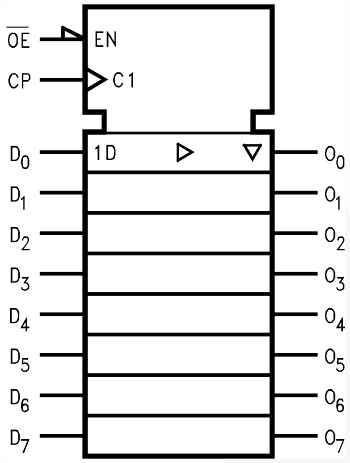
Functional Description

The LVT574 and LVTH574 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Symbols



IEEE/IEC

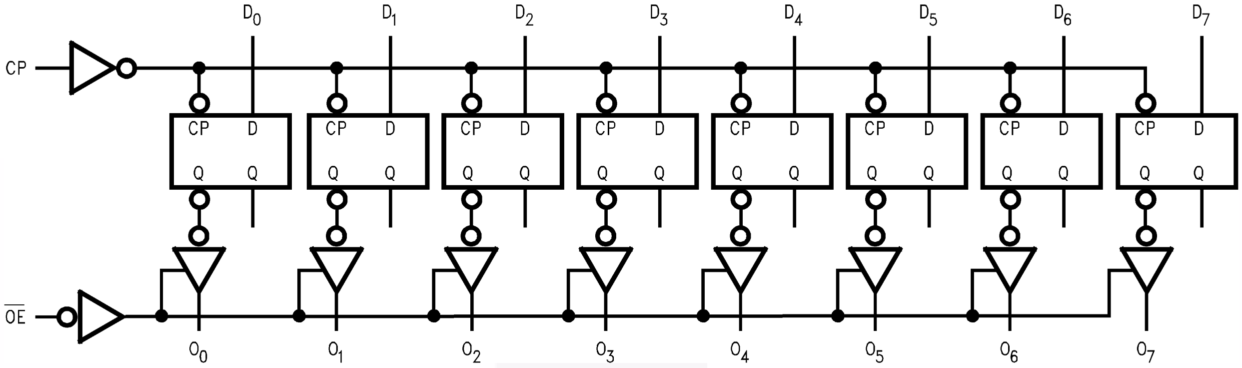


Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	L	L	O_o
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
O_o = Previous O_o before HIGH to LOW of CP

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State$^{(1)}$	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current, V_O < GND	–50mA
I_O	DC Output Current, $V_O > V_{CC}$ Output at HIGH State	64mA
	Output at LOW State	128mA
I_{CC}	DC Supply Current per Supply Pin	±64mA
I_{GND}	DC Ground Current per Ground Pin	±128mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		–32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C			Units
				Min.	Typ.[2]	Max.	
V_{IK}	Input Clamp Diode Voltage	2.7	I_I = –18mA			–1.2	V
V_{IH}	Input HIGH Voltage	2.7–3.6	$V_O \leq$ 0.1V or $V_O \geq V_{CC}$ – 0.1V	2.0			V
V_{IL}	Input LOW Voltage	2.7–3.6				0.8	V
V_{OH}	Output HIGH Voltage	2.7–3.6	I_{OH} = –100µA	V_{CC} – 0.2			V
		2.7	I_{OH} = –8mA	2.4			
		3.0	I_{OH} = –32mA	2.0			
V_{OL}	Output LOW Voltage	2.7	I_{OL} = 100µA			0.2	V
			I_{OL} = 24mA			0.5	
		3.0	I_{OL} = 16mA			0.4	
			I_{OL} = 32mA			0.5	
			I_{OL} = 64mA			0.55	
$I_{I(HOLD)}$[3]	Bushold Input Minimum Drive	3.0	V_I = 0.8V	75			µA
			V_I = 2.0V	–75			
$I_{I(OD)}$[3]	Bushold Input Over-Drive Current to Change State	3.0	[4]	500			µA
			[5]	–500			
I_I	Input Current	3.6	V_I = 5.5V			10	µA
	Control Pins	3.6	V_I = 0V or V_{CC}			±1	
	Data Pins	3.6	V_I = 0V			–5	
			$V_I = V_{CC}$			1	
I_{OFF}	Power Off Leakage Current	0	0V $\leq V_I$ or $V_O \leq$ 5.5V			±100	µA
$I_{PU/PD}$	Power up/down 3-STATE Output Current	0–1.5	V_O = 0.5V to 3.0V, V_I = GND or V_{CC}			±100	µA
I_{OZL}	3-STATE Output Leakage Current	3.6	V_O = 0.5V			–5	µA
I_{OZH}	3-STATE Output Leakage Current	3.6	V_O = 3.0V			5	µA
$I_{OZH}+$	3-STATE Output Leakage Current	3.6	$V_{CC} < V_O \leq$ 5.5V			10	µA
I_{CCH}	Power Supply Current	3.6	Outputs HIGH			0.19	mA
I_{CCL}	Power Supply Current	3.6	Outputs LOW			5	mA
I_{CCZ}	Power Supply Current	3.6	Outputs Disabled			0.19	mA
$I_{CCZ}+$	Power Supply Current	3.6	$V_{CC} \leq V_O \leq$ 5.5V, Outputs Disabled			0.19	mA
ΔI_{CC}	Increase in Power Supply Current[6]	3.6	One Input at V_{CC} – 0.6V, Other Inputs at V_{CC} or GND			0.2	mA

Notes:

2. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
3. Applies to bushold versions only (74LVTH574).
4. An external driver must source at least the specified current to switch from LOW-to-HIGH.
5. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
6. This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics[7]

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$			Units
			$C_L = 50pF, R_L = 500\Omega$	Min.	Typ.	Max.	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	[8]		0.8		V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	[8]		–0.8		V

Notes:

7. Characterized in SOIC package. Guaranteed parameter, but not tested.
8. Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $C_L = 50pF, R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min.	Typ.[9]	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	150			150		MHz
t_{PHL}	Propagation Delay, CP to O_n	1.8		4.6	1.8	5.3	ns
t_{PLH}		1.8		4.5	1.8	5.3	
t_{PZL}	Output Enable Time	1.5		5.2	1.5	6.1	ns
t_{PZH}		1.5		4.8	1.5	5.9	
t_{PLZ}	Output Disable Time	2.0		4.4	2.0	4.4	ns
t_{PHZ}		2.0		4.8	2.0	5.1	
t_S	Setup Time	2.0			2.4		ns
t_H	Hold Time	0.3			0.0		ns
t_W	Pulse Width	3.3			3.3		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew[10]			1.0		1.0	ns

Notes:

9. All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.
10. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

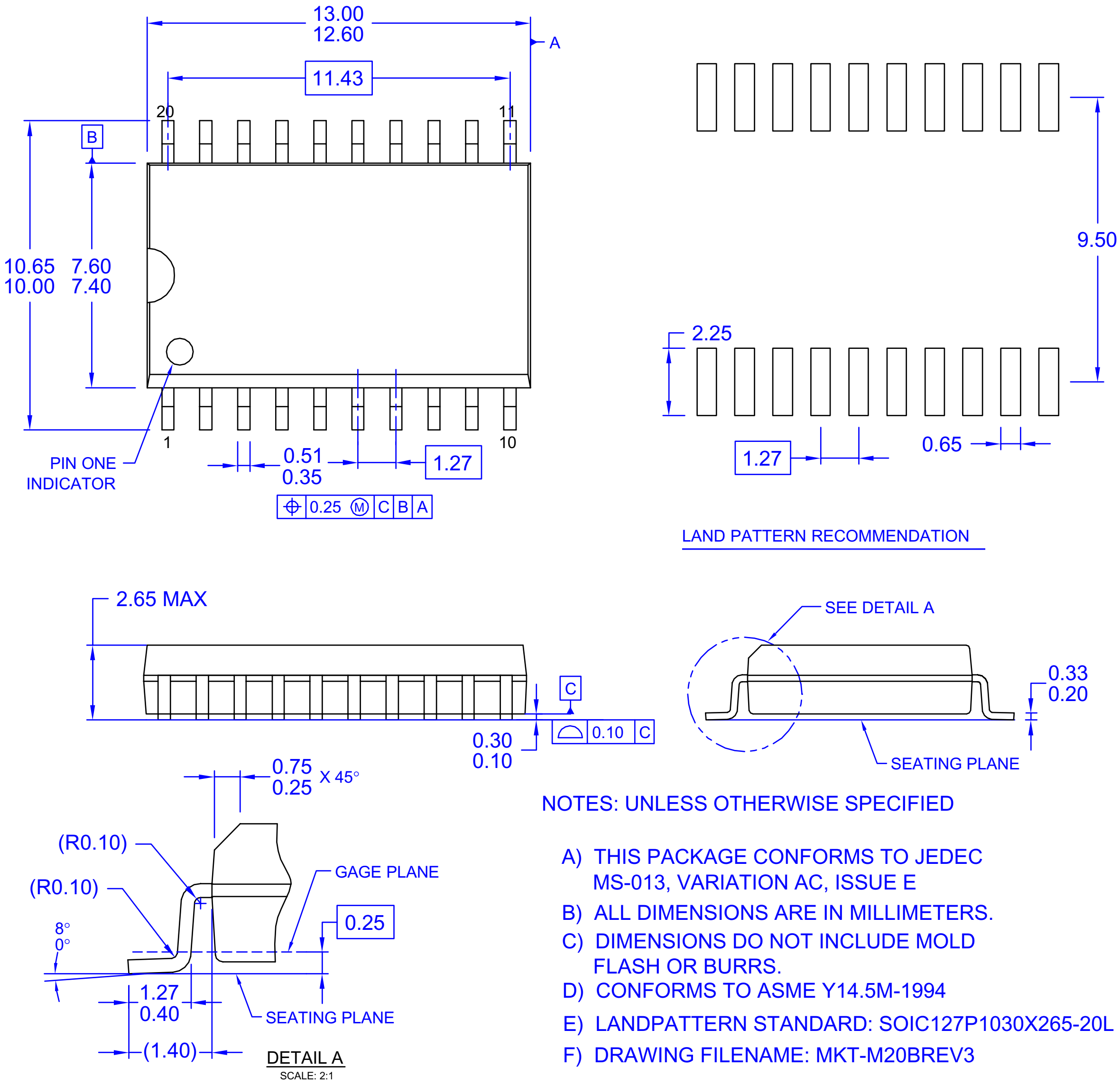
Capacitance[11]

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	6	pF

Note:

11. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-013, VARIATION AC, ISSUE E

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D) CONFORMS TO ASME Y14.5M-1994

E) LANDPATTERN STANDARD: SOIC127P1030X265-20L

F) DRAWING FILENAME: MKT-M20BREV3

Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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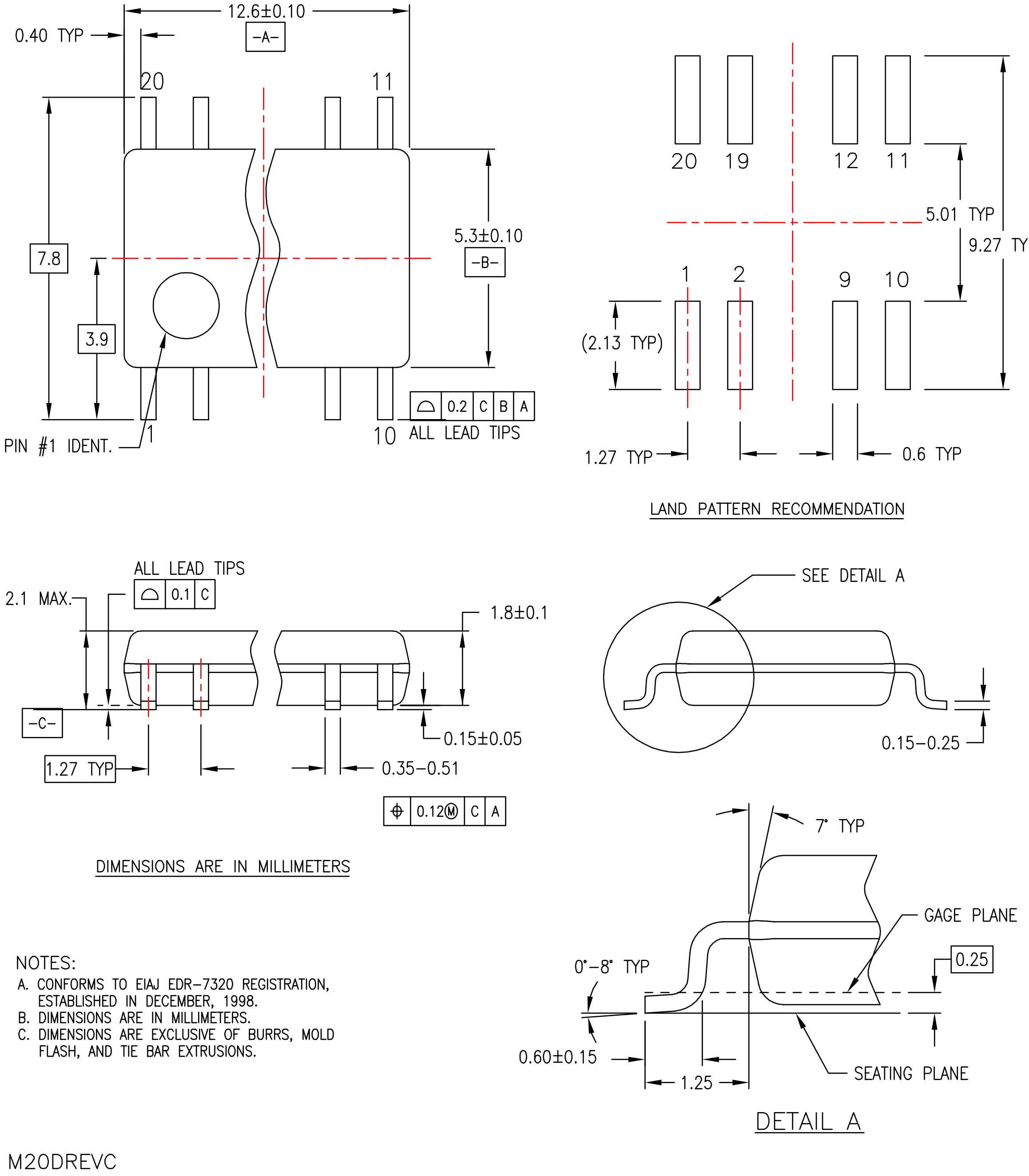
Physical Dimensions (Continued)



NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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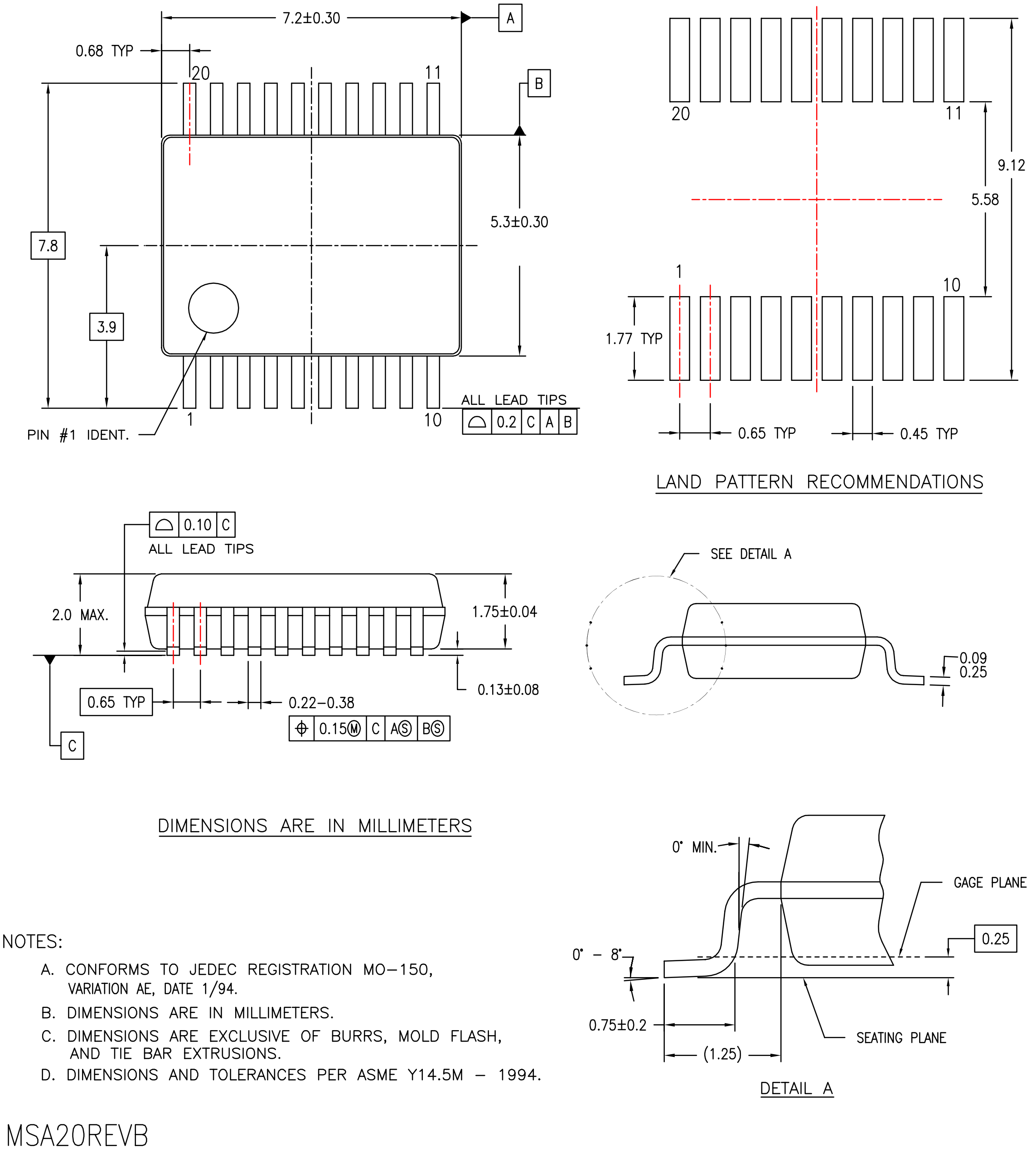
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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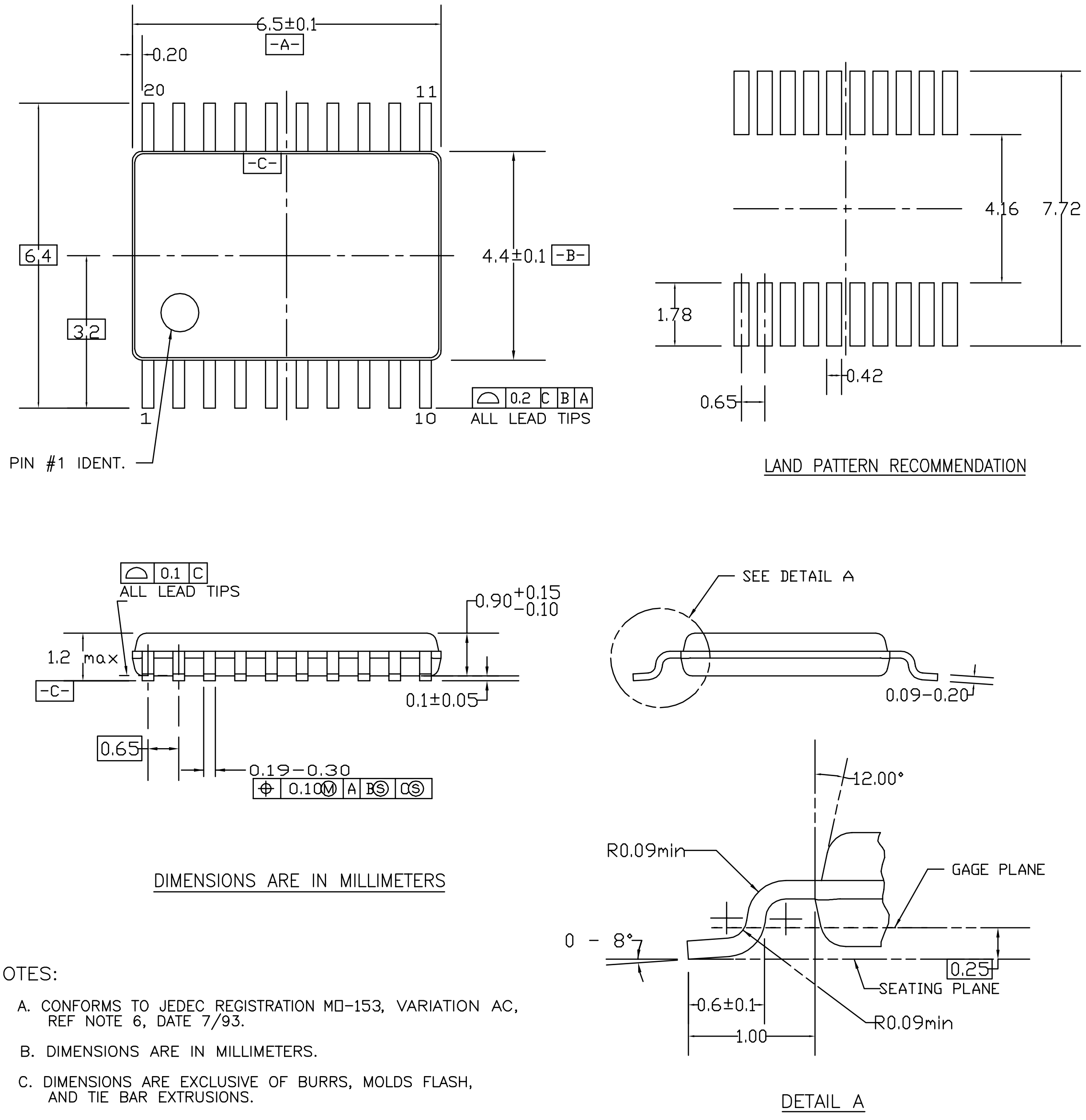
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Rev. I33